cont B1

a low concentration impurity layer having an identical conductivity laminated on the plate of the high concentration impurity layer.

amended B2

3. (Twice Amended) A dielectrically separated wafer having a polysilicon layer and a plurality of monocrystalline silicon islands mutually separated by a dielectrically separating layer consisting of a silicon oxide film which is formed on a surface of a polysilicon layer, wherein:

said polysilicon layer is formed by a seed low temperature CVD polysilicon layer grown by a low temperature CVD method on an interface with said dielectrically separating oxide film and a polysilicon layer formed by a high temperature CVD method.

amended B3

5. (Twice Amended) A dielectrically separated wafer, having a plurality of dielectrically separated monocrystalline silicon islands separated by a dielectrically separating oxide film on the wafer surface, the dielectrically separated wafer comprises a surface between one dielectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat by controlling the separation polishing of monocrystalline silicon and the dielectric layer.

See the attached Appendix for the changes made to effect the above-amended claims.